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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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30827	7590	09/28/2005	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006			LANDAU, MATTHEW C	
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			2815	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/026,961	Applicant(s) HA ET AL.	
	Examiner Matthew Landau	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 10-14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-9, 15-18, 20 and 22 is/are rejected.
- 7) ☒ Claim(s) 5, 19 and 21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 December 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Claims 10-14 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Election was made **without** traverse in the reply filed on 4/11/2003.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation “wherein the storage electrode is directly connected to the pixel electrode on an entire surface of the second region of the storage electrode” (claims 1, 6, and 15) must be shown or the feature(s) canceled from the claim(s). Although Figures 8 and 11 show the pixel electrode 52 overlapping the storage electrode, they do not show exactly where the pixel electrode connects to the second region of the storage electrode. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

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renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 19 objected to because of the following informalities: the limitation "surrounds over the storage electrode" should be changed to "surrounds an area over the storage electrode". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 6-9 are rejected under 35 U.S.C. 102(a) as being anticipated by the admitted prior art.

Regarding claim 6, Figures 4 and 5 of the instant application (the admitted prior art) disclose a liquid crystal display device including a data line 4 supplied with a data signal, a gate line 2 supplied with a scanning signal, a pixel electrode 22 for driving a liquid crystal cell, and a

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thin film transistor T for responding to the scanning signal to switch the data signal to the pixel electrode, the device comprising: a storage electrode 30 having a first region (left side as shown in Figure 5) overlapping the gate line to form a storage capacitor, and a second region (right side as shown in Figure 5) offset and parallel to the gate line; and the pixel electrode covering an upper surface and side edges of the storage electrode, wherein the storage electrode is directly connected to the pixel electrode on an entire surface of the second region of the storage electrode.

Regarding claim 7, Figures 4 and 5 of the admitted prior art disclose the gate line 2 formed on a substrate 1; a gate insulating film 12 formed on the substrate to cover the gate line; and a first semiconductor layer 14 formed on the gate insulating film. The product-by-process limitations “simultaneously patterned with the storage electrode” does not structurally/patentably distinguish the claimed invention over the admitted prior art.

Regarding claim 8, Figures 4 and 5 of the admitted prior art disclose a gate electrode 6 connected with the gate line 2 on said substrate 1; a gate insulating film 12 on said substrate; a second semiconductor layer 14/16 (left side) on said gate insulating film; a source electrode 8 and a drain electrode 10 on said second semiconductor layer; a protective layer 18 on said gate insulating film; and the pixel electrode 22 on said protective layer.

Regarding claim 9, Figure 5 of the admitted prior art discloses the second semiconductor layer 14/16 includes an active layer 14 and an ohmic contact layer 16. The limitations “the active layer being patterned simultaneously with...” and “the ohmic contact layer being patterned simultaneously with...” are product-by-process limitations that do not structurally/patentably distinguish the claimed invention over the admitted prior art.

Claims 1-4, 6-8, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US Pat. 6,091,466, hereinafter Kim'466).

Regarding claim 1, Figures 4 and 5F of Kim'466 disclose a liquid crystal display device including a data line 123 supplied with a data signal, a gate lines 113 supplied with a scanning signal, a pixel electrode 141 for driving a liquid crystal cell, and a thin film transistor for responding to the scanning signal to switch the data signal to the pixel electrode, the device comprising: a storage electrode 151 having a first region (right side as shown in Figure 5F) overlapping the gate line to form a storage capacitor, and a second region (left side as shown in Figure 5F) offset and parallel to the gate line; a first protective layer 137 having non-contiguous portions at respective ends of the storage electrode in a layer between the storage electrode and the pixel electrode, wherein the storage electrode is directly connected to the pixel electrode on an entire surface of the second region of the storage electrode in areas not including the first protective layer; and a second protective layer 137 formed between a gate insulating film 117 and the pixel electrode (portion of 137 between drain electrode 131 and pixel electrode 141). Note that the portions of protective layer 137 above the first and second regions of the storage electrode (right and left sides) (as shown in Figure 5F) are not directly touching. Therefore, at least these portions can be considered "non-contiguous". Also note that Kim'466 discloses the protective layer 137 is formed on the entire structure and then a contact hole 181 is formed for the storage electrode (col. 6, lines 11-15). Therefore, the only portion of the storage electrode that is not covered with the protective layer 137 is the portion that is in contact with the pixel

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electrode through the contact hole 181. In other words, the surface of the second region not including the first protective layer is directly connected to the pixel electrode.

Regarding claim 2, Figure 5F of Kim'466 discloses the gate insulating film 117 on a substrate 101 in such a manner to cover the gate line; and a first semiconductor layer 133a/135a between the gate insulating film and the storage electrode.

Regarding claim 3, Figure 5F of Kim'466 discloses the first protective layer 137 is formed at side edges of the storage capacitor.

Regarding claim 4, Figures 4 and 5F of Kim'466 disclose a gate electrode 111 contacting the gate line 117 on the substrate 101; a second semiconductor layer 133/135 on the gate insulating film; and a source electrode 121 and a drain electrode 131 on the second semiconductor layer.

Regarding claim 6, Figures 4 and 5F of Kim'466 disclose a liquid crystal display device including a data line 123 supplied with a data signal, a gate lines 113 supplied with a scanning signal, a pixel electrode 141 for driving a liquid crystal cell, and a thin film transistor for responding to the scanning signal to switch the data signal to the pixel electrode, the device comprising: a storage electrode 151 having a first region (right side as shown in Figure 5F) overlapping with the gate line to form a storage capacitor, and a second region (left side as shown in Figure 5F) offset and parallel to the gate line; and the pixel electrode 141 covering an upper surface and side edges of the storage electrode (Figure 5F), wherein the storage electrode is directly connected to the pixel electrode on an entire surface of the second region of the storage electrode. It is considered that "an entire surface" is the surface not covered by the protective layer 137 (i.e., the surface exposed in contact hole 181) (see rejection of claim 1).

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Note that Applicant has not defined what surface of the second region the limitation “an entire surface” refers to.

Regarding claim 7, Figures 4 and 5F of Kim’466 disclose the gate line 113 formed on a substrate 101; a gate insulating film 117 formed on the substrate to cover the gate line; and a first semiconductor layer 135a formed on the gate insulating film. The product-by-process limitation “simultaneously patterned with the storage electrode” does not structurally/patentably distinguish the claimed invention over Kim’466.

Regarding claim 8, Figures 4 and 5F of Kim’466 disclose a gate electrode 111 connected with the gate line 113 on said substrate 101; a gate insulating film 117 on said substrate; a second semiconductor layer 133/135 on said gate insulating film; a source electrode 121 and a drain electrode 131 on said second semiconductor layer; a protective layer 137 on said gate insulating film; and the pixel electrode 141 on said protective layer.

Regarding claim 20, the product-by-process limitation “wherein the first protective layer is simultaneously formed...” does not structurally/patentably distinguish the claimed invention over Kim’466.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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Claims 15-18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim'466 in view of Kim (US Pat. 6,262,784, hereinafter Kim'784).

Regarding claim 15, as best the examiner can ascertain the claimed invention, Figures 4 and 5F of Kim '466 disclose a first substrate 101; a gate line 113 and a data line 123 over the substrate, the data line crossing the gate line to define a pixel region; a thin film transistor having source and drain electrodes (131 and 121) at the crossing of the gate line and data line; a storage electrode 151 having a first region (right side as shown in Figure 5F) over the gate line, and a second region (left side as shown in Figure 5F) offset and parallel to the gate line; a pixel electrode 141 over the storage electrode; a first protective layer 137 having non-contiguous portions at respective ends of the storage electrode in a layer between the storage electrode and the pixel electrode, wherein the pixel electrode directly connects to the storage electrode on an entire surface of the second region in areas not including the first protective layer; a second protective layer 137 formed between a gate insulating film 117 and the pixel electrode (portion of 137 between drain electrode 131 and pixel electrode 141). Note that the portions of protective layer 137 above the first and second regions of the storage electrode (right and left sides) (as shown in Figure 5F) are not directly touching. Therefore, at least these portions can be considered "non-contiguous". Also note that Kim'466 discloses the protective layer 137 is formed on the entire structure and then a contact hole 181 is formed for the storage electrode (col. 6, lines 11-15). Therefore, the only portion of the storage electrode that is not covered with the protective layer 137 is the portion that is in contact with the pixel electrode through the contact hole 181. In other words, the surface of the second region not including the first protective layer is directly connected to the pixel electrode. Kim'466 does not explicitly disclose

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a second substrate with a liquid crystal layer between the first and second substrates. Figure 3 of Kim'784 discloses a liquid crystal layer 190 formed between first and second substrates (100 and 200). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kim'466 for the purpose obtaining a fully functional liquid crystal display device.

Regarding claim 16, Figure 4 of Kim'466 discloses the pixel electrode 141 surrounds an area over the storage electrode.

Regarding claim 17, Figure 5F of Kim'466 discloses a storage capacitor is formed between the storage electrode 151 and the gate line 113 and wherein the first protective layer 137 overlaps a portion of the storage capacitor.

Regarding claim 18, Figure 5F of Kim'466 discloses a storage capacitor is formed between the storage electrode 151 and the gate line 113 and wherein the first protective layer 137 overlaps a lower edge of the storage capacitor.

Regarding claim 22, the product-by-process limitation "wherein the first protective layer is simultaneously formed..." does not structurally/patentably distinguish the claimed invention over Kim'466.

Allowable Subject Matter

Claims 5, 19, and 21 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 5 and 21, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including the active layer is patterned simultaneously with the second protective layer and the ohmic contact layer is patterned simultaneously with the source electrode and the drain electrode.

Regarding claim 19, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including the pixel electrode is substantially rounded where the pixel electrode surrounds over the storage electrode.

Response to Arguments

Applicant's arguments filed July 14, 2005 have been fully considered but they are not persuasive.

Applicant argues that, "Kim '466 fails to teach or suggest a liquid crystal display device "wherein the storage electrode is directed connected to the pixel electrode on an entire surface of the second region of the storage electrode in areas not including the first protective layer"". As explained in the rejection of claim 1 above, Kim'466 discloses the protective layer 137 is deposited over the entire device and then a contact hole 181 is formed for the storage electrode. The only portions of the storage electrode that are not covered by the layer 137 are those in the contact hole, which are in direct contact with the pixel electrode 141. Therefore, the pixel electrode of Kim'466 is directly connected to storage electrode on an entire surface of the second region in areas not including the first protective layer. Applicant makes similar arguments regarding claim 6. As explained in the above rejection, Applicant has not defined which surface of the second region "an entire surface" refers to. Therefore, it can be considered that "an entire

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surface” is the surface of the second region not covered by layer 137. As explained above and shown in Figure 5F of Kim’466, the surface of the storage electrode not covered by layer 137 is directly connected to the pixel electrode 141. Therefore, Applicant’s arguments are not persuasive and the claims are anticipated.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Matthew C. Landau

September 26, 2005